AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 2, 12 and 19 without prejudice.

1. (CURRENTLY AMENDED) A device comprising:

a demodulator circuit configured to generate (i) a first clock signal compliant with a standard interface for a digital video receiver and (ii) a first plurality of data signals compliant with said standard interface;

a decoder circuit configured to receive a second plurality of data signals compliant with said standard interface;

a plurality of first bi-directional buffers configured to multiplex said first data signals with said second data signals at a plurality of data interfaces in response to said first clock signal; ~~and~~

a circuit configured to generate a direction signal at a direction interface in response to said first clock signal to indicate a direction of said data interfaces; and

a delay circuit configured to generate a second clock signal compliant with said standard interface by phase shifting said first clock signal.

2. (CANCELED)

3. (CURRENTLY AMENDED) The device according to claim ~~2~~ 1, wherein said second data signals are ready to be read at an edge of said second clock signal.

4. (CURRENTLY AMENDED) The device according to claim ~~2~~ 1, wherein said delay circuit is further configured to generate a third clock signal compliant with said standard interface at a clock interface by phase shifting said first clock signal.

5. (CURRENTLY AMENDED) The device according to claim ~~3~~ 4, wherein said first data signals are ready to be read at an edge of said third clock signal.

6. (ORIGINAL) The device according to claim 1, further comprising a second bi-directional buffer configured to multiplex a first valid signal compliant with said standard interface with a second valid signal compliant with said standard interface at a valid interface in response to said first clock signal, said first valid signal indicating when said first data signals are valid and said second valid signal indicating when said second data signals are valid.

7. (ORIGINAL) The device according to claim ~~6~~ 5, further comprising a third bi-directional buffer configured to multiplex a

first synchronization signal compliant with said standard interface with a second synchronization signal compliant with said standard interface at a synchronization interface in response to said first clock signal, said first synchronization signal indicating a first start of packet for said first data signal and said second synchronization signal indicating a second start of packet for said second data signals.

8. (ORIGINAL) The device according to claim 1, wherein said demodulator circuit is further configured to generate an error signal at an error interface to indicate a demodulation error.

9. (ORIGINAL) The device according to claim 8, further comprising:

a delay circuit configured to generate a second clock signal compliant with said standard interface, wherein said second data signals are ready to be read at an edge of said second clock signal;

a second bi-directional buffer configured to multiplex a first valid signal compliant with said standard interface with a second valid signal compliant with said standard interface at a valid interface in response to said first clock signal, said first valid signal indicating when said first data signals are valid and

said second valid signal indicating when said second data signals are valid; and

a third bi-directional buffer configured to multiplex a first synchronization signal compliant with said standard interface with a second synchronization signal compliant with said standard interface at a synchronization interface in response to said first clock signal, said first synchronization signal indicating a first start of packet for said first data signal and said second synchronization signal indicating a second start of packet for said second data signals.

10. (ORIGINAL) The device according to claim 9, wherein said standard interface comprises European Standard reference number EN 50221.

11. (CURRENTLY AMENDED) A method of transferring data defined by a standard interface for a digital video receiver comprising the steps of:

(A) generating a first clock signal compliant with said standard interface;

(B) multiplexing a first plurality of data signals compliant with said standard interface with a second plurality of data signals compliant with said standard interface at a plurality of data interfaces in response to said first clock signal; ~~and~~

(C) generating a direction signal at a direction interface in response to said first clock signal to indicate a direction of said data interfaces; and

(D) generating a second clock signal compliant with said standard interface in response to phase shifting said first clock signal.

12. (CANCELED)

13. (CURRENTLY AMENDED) The method according to claim ~~12~~ 11, wherein said second data signals are ready to be read at an edge of said second clock signal.

14. (CURRENTLY AMENDED) The method according to claim ~~12~~ 11, further comprising the step of generating a third clock signal compliant with said standard interface at a clock interface in response to phase shifting said first clock signal.

15. (ORIGINAL) The method according to claim 14, wherein said first data signals are ready to be read at an edge of said third clock signal.

16. (ORIGINAL) The method according to claim 11, further comprising the step of multiplexing a first valid signal compliant

with said standard interface with a second valid signal compliant with said standard interface, said first valid signal indicating when said first data signals are valid and said second valid signal indicating when said second data signals are valid.

17. (ORIGINAL) The method according to claim 16, further comprising the step of multiplexing a first synchronization signal compliant with said standard interface with a second synchronization signal compliant with said standard interface in response to said first clock signal, said first synchronization signal indicating a first start of packet for said first data signal and said second synchronization signal indicating a second start of packet for said second data signals.

18. (ORIGINAL) The method according to claim 11, further comprising the step of generating an error signal at an error interface to indicate a demodulation error.

19. (CANCELED)

20. (NEW) A device comprising:

a demodulator circuit configured to generate (i) a first clock signal compliant with a standard interface for a digital

video receiver and (ii) a first plurality of data signals compliant with said standard interface;

a decoder circuit configured to receive a second plurality of data signals compliant with said standard interface;

a plurality of first bi-directional buffers configured to multiplex said first data signals with said second data signals at a plurality of data interfaces in response to said first clock signal; and

a circuit configured to generate a direction signal at a direction interface in response to said first clock signal to indicate a direction of said data interfaces, wherein said demodulator circuit is further configured to generate an error signal at an error interface to indicate a demodulation error.